WHAT IS CLAIMED IS:

1. A memory unit including a memory device having at least one of a data unit and a semiconductor memory chip having a management unit corresponding to said data unit,

wherein said memory device is divided into a plurality of memory areas, management information capable of controlling separately each of said memory areas for accessing from outside is tabled in said data unit, and control information for setting a limit to accessing a prescribed memory area of said plural memory areas is included in said management information.

2. A memory unit including a memory device having at least one of a data unit and a semiconductor memory chip having a management unit corresponding to said data unit,

wherein said memory device is divided into a plurality of memory areas, management information capable of controlling separately each of said memory areas for accessing from outside is tabled in said data unit,

wherein said management information includes at least one of first to fourth information, said first control information prohibiting writing data in a prescribed memory area of said plural memory areas, said second control information prohibiting reading out data from a prescribed memory area of said plural memory areas, said third control information being capable of performing simultaneously mirroring for storing data which are

written in a prescribed memory area of said plural memory areas in a plurality of places at a same time, and said fourth control information being capable of time difference mirroring for storing data which are written in a prescribed memory area of said plural memory areas in plural places after a prescribed time has passed.

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3. A memory unit according to claim 2, wherein said management information includes fifth control information for identifying whether or not a memory area which is kept as a spare area in advance is capable of being used.

4. A memory unit according to claim 3, wherein said management information includes sixth control information for indicating erasing number of times or rewriting number of times of a memory area.

5. A memory unit according to claim 4, wherein a memory means for storing said management information altogether is included.

6. A memory unit according to claim 4, wherein an area for storing said management information by each memory area is provided in said plural memory areas.

7. A memory unit according to claim 6, wherein control means for controlling separately said memory area based on said management information is included.

8. A memory unit according to claim 7, wherein said control means includes a micro processing unit for processing said management information by software.

9. A memory unit according to claim 7, wherein said control means includes a controlling unit for processing said management information by exclusive hardware.

10. A data processing system according to claim 9, wherein a memory unit and a host device capable of accessing it are included.

11. A data processing system according to any one of claims 1 to 6, wherein a memory unit and a host device capable of accessing it are included and said host device includes an information processing unit for controlling separately said memory area based on said management information.

12. A method for controlling a memory device including at least one semiconductor memory chip having a data unit and a management unit corresponding to said data unit,

wherein, when said memory device is divided into plural memory areas, the method comprises a step for controlling separately said memory device by each memory area based on management information that is tabled on said data unit, by including at least one of first to fourth control information, said first control information prohibiting writing data in a prescribed memory area of said plural memory areas, said second control information prohibiting reading out data from a prescribed memory area of said plural memory areas, said third control information storing data that are written in a prescribed memory area of said plural memory areas in plural places nearly at a same time, and said fourth control information storing data

that are written in a prescribed memory area of said plural memory areas in plural places after a prescribed time has passed.

13. A method for controlling a memory device according to claim 12, wherein said management information includes fifth control information for identifying whether or not a memory area is usable.

14. A method for controlling a memory device according to claim 13, wherein said management information includes sixth control information for indicating erasing number of times and rewriting number of times of a memory area.

15. A method for controlling a memory device according to claim 14, wherein said method includes a first step having a management information edit step capable of editing said management information and identifying whether or not said step of editing said management information transits to an edit mode of said management information and a second step for editing said management information in an edit mode which is transited based on an identifying result at said first step.

16. A method for controlling a memory device according to claim 15, wherein said second step includes:

a third step for identifying whether or not a command given from a host device is a writing command to a random access memory from said host device and for writing said management information in said random access memory from said host device based on an identified result thereof,

a fourth step for identifying whether or not a command given from said host device is a command for writing a memory device from said random access memory and writing said management information in said memory device from said random access memory,

a fifth step for identifying whether or not a command given from said host device is a command for reading out to said random access memory from said memory device and reading out said management information to said random access memory from said memory device, and

a sixth step for identifying whether or not a command given from said host device is a command for reading out said host unit from said random access memory and reading out said management information to said host device from said random access memory.